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METHOD OF PROGRAMMING PLDS USING A WIRELESS LINK

Field of the Invention

The present invention relates to a method and/or architecture for programming programmable logic devices (PLDs) generally and, more particularly, to a method and/or architecture for programming PLDs using a wireless link.

Background of the Invention

Programmable logic devices (PLDs) that can be programmed and reprogrammed without being removed from an application environment are needed in many applications. Programming a PLD is typically achieved by transferring a bit pattern into the programmable logic device. The bit pattern determines the arrangement and operation of resources in the programmable logic device. The process of designing with PLDs includes fitting a design to a device by determining the required resources and timing. A programming file is then generated that contains the required bit pattern for the PLD.

A reprogrammable system can be reprogrammed by a host programming device. Programming instructions can be communicated over a hard-wired (physical) or a wireless connection. Most devices are currently programmed in system using a cable or other physical connection to the host. A system that uses a wireless link may be found in U.S. Patent 6,023,570, which is hereby incorporated by reference in its entirety. The wireless system requires a microprocessor connected to a wireless transceiver and to a number of PLDs on a printed circuit board (PCB). A personal computer (PC) or workstation ATE tester sends data to the microprocessor over the wireless link. The microprocessor then programs the PLDs. When programming is completed, the microprocessor and wireless transceiver serve no other function.

A disadvantage of such a conventional wireless system is that additional hardware is required. The additional hardware includes a printed circuit board containing the number of PLDs, a programmer, and an access interface (i.e., a serial or parallel port interface) that connects the programmer to a host controller over the communication link. The conventional programmer contains a microprocessor, a random access memory (RAM), a non-volatile memory (i.e., EPROM), and a number of signal latches.

A PLD that could be programmed and reprogrammed using a wireless link without requiring additional hardware or removal from a system would be very useful.

Summary of the Invention

The present invention concerns an apparatus comprising a wireless transceiver and a programmable logic circuit. The wireless transceiver may be coupled to the programmable logic circuit. The programmable logic circuit may comprise a memory circuit, a processor, and a programmable logic device implemented in a single integrated circuit package.

The objects, features and advantages of the present invention include providing a method and/or architecture for programming a programmable logic device (PLD) using a wireless link that may (i) require minimal additional hardware, (ii) include a microprocessor, micro-controller, or digital signal processor (DSP) functionality, (iii) reduce component count and printed circuit board area requirements, (iv) be less expensive to implement than conventional approaches and/or (v) not require extra die area compared with conventional approaches.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a preferred embodiment of the present invention;

FIG. 2 is a block diagram of a preferred embodiment of the present invention;

FIG. 3 is a block diagram of an alternative embodiment of the present invention; and

FIG. 4 is a block diagram of another alternative embodiment of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented, in one example, as a programmable logic device (PLD) that may be programmed and/or reprogrammed while in a system, using a wireless link. The circuit 100 may implement the wireless link using a wireless protocol. In one example, the wireless protocol may be implemented in accordance

with the Bluetooth™ protocol (Bluetooth is a trademark of Telefonakiebolaget LM Ericsson, Stockholm Sweden). A description of the Bluetooth™ protocol may be found in the BLUETOOTH SPECIFICATION version 1.0A, published July 24, 1999 (revised December 1, 1999), which is hereby incorporated by reference in its entirety.

The wireless link may comprise, in one example, radio waves, infrared or other wavelength light, ultrasonic waves, and/or any other media of communication that generally do not require a physical connection. The present invention may provide a single chip solution (or a multiple chip solution within one integrated circuit package) that may be less expensive to implement and may require less hardware, compared with previous solutions. A PLD implemented in accordance with the present invention may reduce printed circuit board area requirements of a system.

The circuit 100 may comprise a circuit 102, a circuit 104 and a transducer 106. The circuit 102 may be implemented, in one example, as a single chip wirelessly programmable PLD. For example, the circuit 102 may be implemented on a single integrated circuit. Alternatively, the circuit 102 may be implemented on multiple integrated circuits as a multi-chip module (MCM). The

individual integrated circuits or dies may be encased in a single integrated circuit package.

The circuit 104 may be implemented, in one example, as a wireless transceiver circuit. The transducer 106 may be implemented, in one example, as a device that may couple a host system and the circuit 104 via a wireless medium. For example, the transducer 106 may be an antenna, an infrared (or other wavelength of light) device (e.g., a light emitting diode (LED) and/or a photo transistor), or an ultrasonic transducer. However, other types of transducers may be implemented accordingly to meet the design criteria of a particular application.

The circuits 102 and 104 may be implemented, in one example, as a multi-chip module with two or more integrated circuits mounted in a single integrated circuit package. In one example, the transducer 106 (e.g., a radio frequency antenna, etc.) may also be included in the single integrated circuit package with the circuit 102 and the circuit 104.

The circuit 102 may have an input/output 108 that may be connected to an input/output 110 of the circuit 104. In general, signals may be received from, or sent to, a host system 111 by the circuit 102 via the circuit 104 and the transducer 106. The

circuit 102 may be configured, in one example, to (i) perform a reprogramming operation in response to signals received from the host system via the wireless link and/or (ii) verify completion and/or success of the programming operation by presenting signals to the host system via the wireless link.

Referring to FIG. 2, a block diagram illustrating an implementation of the circuit 100 in accordance with the present invention is shown. The circuit 102 may be implemented, in one example, as a microprocessor, micro-controller, or digital signal processor in a single package with a PLD and/or memory. The circuit 102 may comprise, in one example, a programmable logic device 112, a memory circuit 114, and a processor circuit 116. The PLD 112 may be implemented, in one example, using currently existing programmable logic devices. The memory circuit 114 may be implemented, in one example, as a non-volatile memory (e.g., FLASH memory, EPROM, EEPROM, etc.). However, other types of non-volatile memory may be implemented accordingly to meet the design criteria of a particular application. The processor circuit 116 may be implemented, in one example, as a microprocessor (μP), a micro-controller (μC), a digital signal processor (DSP), or other appropriate processor. The processor circuit 116 may be

configured, in one example, to (i) communicate with a host system via the wireless transceiver 104 and (ii) program either the PLD 112 or the memory circuit 114 in response to signals from the wireless transceiver 104. The memory circuit 114 may be configured to store configuration data received from the processor 116. The configuration data stored in the memory circuit 114 may be used for programming the PLD 112 upon bootup. The PLD 112 may be connected to the processor 116 by a bidirectional bus. The PLD 112 may be configured, in one example, to communicate with and/or control the processor 116. In one example, the functionality of the PLD 112 may be augmented by the additional functionality of the processor 116 alone or in combination with the wireless transceiver 104.

The PLD 112, the memory circuit 114 and the processor circuit 116 may be implemented, in one example, on individual silicon dies. The individual dies may be encased together in a single integrated circuit package. The package may be, in one example, an integrated circuit package in accordance with the JEDEC standard. Alternatively, the integrated circuit package may be a multi-chip module.

Referring to FIG. 3, a block diagram of a circuit 100′ illustrating an alternative embodiment of the present invention is

shown. The circuit 100′ may be implemented similarly to the circuit 100 except that the circuit 100′ may comprise a circuit 102′. The circuit 102′ may be implemented using a first and a second die. The first die may contain a memory circuit 114′ and the second die may contain both a PLD 112′ and a processor 116′. By implementing the PLD 112′ and the processor 116′ on a single die, the circuit 102′ may provide for easier and less expensive packaging. The memory circuit 114′ may be implemented similarly to the memory circuit 114 described above in connection with FIG. 2. The processor 116′ may be implemented as a microprocessor, a micro-controller, a digital signal processor, or other appropriate processor. The PLD 112′ and processor 116′ may be configured, in one example, so that the PLD 112′ may access the transceiver 104 through the processor 116′. The use of the processor 116′ to access the transceiver 104 may be transparent to the PLD 112′. Alternatively, the PLD 112′ may access all control, input/output, and other appropriate pins of the processor 116′ as if they were resources accessible to a user from within the design. In one example, the processor may be initiated and used as a functional block in the design. In another alternative, the PLD 112′ may

bypass the processor 116′ (e.g., the processor may appear transparent) to access the transceiver 104 and/or memory 114′.

Upon bootup, the memory 114′ may be configured to program the PLD 112′. The processor 116′ may be configured to program the memory 114′ in response to signals from the wireless transceiver 104. The processor 116′ may present signals to the wireless transceiver 104 that may indicate a status of the programming operation. When the circuit 100′ is rebooted, the new programming in the memory 114′ may reconfigure the PLD 112′.

Referring to FIG. 4, a block diagram of a circuit 100″ illustrating another alternative embodiment of the present invention is shown. The circuit 100″ may be implemented similarly to the circuit 100 except that the circuit 100″ may comprise a circuit 102″. The circuit 102″ may comprise a PLD 112″ and a memory circuit 114″. The memory circuit 114″ may be implemented similarly to the memory circuit 114 described above in connection with FIG. 2. The circuit 100″ may comprise a die containing the memory circuit 114″ and a die containing the PLD 112″. When the circuit 100″ is manufactured, the circuit 100″ may incorporate a microprocessor, micro-controller, a digital signal processor, or other appropriate functionality into the memory 114″ or other

memory that may be on the PLD die (e.g., mask programmable ROM or other memory type). The memory on the PLD die may be implemented, in one example, as any type of non-volatile or one-time programmable memory. The memory circuit 114″ may be programmed when the device is leaving the factory with instructions for configuring the PLD 112″ to operate as the microprocessor, the micro-controller, the digital signal processor, or other appropriate functionality.

Upon a first bootup, the PLD 112″ may be configured as the microprocessor, the micro-controller, the digital signal processor, etc., in response to the instructions stored in the memory 114″. When the PLD 112″ is configured as a microprocessor (or other processor configuration), the PLD 112″ may communicate with the wireless transceiver 104 to receive data for reprogramming the memory circuit 114″ with a desired configuration for the PLD 112″. The new programming in the memory 114″ may reconfigure the PLD 112″ during subsequent bootups.

The present invention may combine a programmable logic device with a processor. Alternatively, the processor may comprise a memory containing instructions for configuring the PLD as a processor. When the present invention is implemented with a

separate PLD and processor, the PLD may be configured to implement logic circuits that may take advantage of the separate microprocessor for enhanced functionality. In one example, the wireless transceiver and transducer may be used to provide input and output to the PLD. A PLD implemented in accordance with the present invention may be programmed or reprogrammed without (i) being removed from a system or (ii) requiring a physical connection to the programming system.

The present invention may provide a method and/or architecture for programming a programmable logic device (PLD) using a wireless link that may (i) require minimal additional hardware, (ii) provide a PLD that includes a microprocessor, a micro-controller, a digital signal processor (DSP), or other processor functionality, (iii) reduce component count and printed circuit board area requirements, (iv) be less expensive to implement than conventional approaches and/or (v) require no extra die area compared with conventional approaches.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes

in form and details may be made without departing from the spirit and scope of the invention.